Remarks:

The Examiner is thanked for the courtesies extended during the in-person interview conducted between the Examiner, the undersigned, and one of the inventors, Ronald Indeck, on February 18, 2011. During this interview, Applicant discussed the claimed invention and its patentable distinctions over the cited references as explained below.

At the time of the outstanding Office Action, the pending claims in the application were claims 40-52, 54-64, and 98-175. By this response, Applicant has (1) amended independent claims 40, 54, 100, and 102 as suggested by the Examiner, and (2) amended dependent claims 41, 47-50, 55, 57, 60-64, 98-99, 103-104, 123-126, 131, 134-138, 141-142, 159-162, and 165 in view of the amendments made to independent claims 40, 54, 100, and 102. No new matter is present. The pending claims remain claims 40-52, 54-64, and 98-175.

The outstanding Office Action also identified claims 51 and 52 as allowed and further identified claims 44, 45, 55-58, 126, 127, 138, and 162 as being allowable if re-written into independent form. Because Applicant respectfully submits that independent claims 40, 54, 100, and 102 are patentable as set forth above, Applicant has not amended those claims into independent form in this response. Applicant thanks the Examiner for his consideration of these claims.

As noted, following the interview, Applicant hereby amends independent claims 40, 54, 100, and 102 as suggested by the Examiner. In particular, these claims now provide stronger antecedent basis for the pipelined data processing engines that reside in the pipeline on the reconfigurable logic device.

The outstanding Office Action rejected independent claims 40, 54, 100, and 102 for alleged obviousness based on the Dixon and Villasenor references. In particular, the Office Action relied on the Villasenor reference for alleged teachings relating to the multi-functional nature of the pipeline claimed in claims 40, 54, 100, and 102. However, as discussed during the interview, the Villasensor reference teaches that the function of its disclosed FPGA (an automatic target recognition (ATR) system) should be changed by reconfiguring the FPGA with a new configuration bitfile corresponding to templates that one wishes to add to the FPGA. By contrast, claims 40, 54, 100, and 102 recite a multi-functional pipeline on a re-configurable logic device wherein the pipelined data processing engines in the pipeline can be activated/deactivated in response to control signals to thereby define the pipeline's function. Thus, the invention of claims 40, 54, 100, and 102 is able to change the pipeline's function by

selectively activating/deactivating the pipelined data processing engines already instantiated on the re-configurable logic device. This means that, with the invention of claims 40, 54, 100, and 102, the hardware logic for a deactivated pipelined data processing engine remains in the pipeline. However, under the teachings of Villasensor, when Villasenor wants to change the FPGA's function from one set of adder trees (corresponding to a first set of templates) to another set of adder trees (corresponding to a second set of templates), Villasenor teaches that the first set of adder trees should be removed from the FPGA (while the second set of adder trees are added to the FPGA). The invention of claims 40, 54, 100, and 102, by contrast, is able to change the pipeline's function in a manner that avoids the time-consuming act of loading a new configuration bitfile onto the re-configurable logic device. As such, it is expected that the invention of claims 40, 54, 100, and 102 will provide lower latency when changing from one pipeline function to another relative to the Dixon/Villasenor combination.

In view of this patentable distinction over the cited references, Applicant respectfully submits that claims 40, 54, 100, and 102 (and all claims depending therefrom) are patentable.

Conclusion:

For the foregoing reasons, Applicant respectfully submits that all pending claims are in condition for allowance.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided below.

Furthermore, Applicant believes that this amendment and remarks are sufficient for overcoming the rejections raised by this Office Action. However, should Applicant later need to further respond to these or new claim rejections, Applicant reserves the right to fully respond to these and any other new rejections, including but not limited to further amending the claims and/or adding new claims, submitting evidence in favor of the patentability of the claims, disputing the alleged prior art status of the cited references if warranted, and raising new arguments in favor of patentability. Moreover, in submitting this response, Applicant does not acquiesce to any characterizations of the claims or art (including any characterizations about what is allegedly known in the art) made in the outstanding Office Action.

A speedy and favorable action is respectfully requested.

Respectfully submitted,

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